AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0006] A multiple mode clock receiver according to an embodiment of the present invention includes first and second input AC-coupled capacitors, first and second voltage dividers and a differential amplifier. The first and second input AC-coupled capacitors include first and second N-channel devices, respectively, each having a source and a drain coupled together at respective input and a gate coupled to a corresponding one of a first junction and a second junction. The voltage dividers are each coupled between DC source voltages (e.g., VDD and ground) and ~~include~~ include the first and second junctions, respectively, coupled to the first and second AC-coupled capacitors, respectively. The differential amplifier has a first input coupled to the first junction and a second input coupled to the second junction. The differential amplifier has an output providing an output clock signal that is aligned with an input clock signal provided through at least one of the input AC-coupled capacitors.

[0007] The multiple mode clock receiver is a single circuit that aligns the output clock signal to any one of multiple forms of input clock signals, such as those prevalently used in existing microprocessor motherboards. A first form is a sole single-ended clock signal provided through the first AC-coupled capacitor. A second form is a single-ended clock signal and a corresponding reference signal provided through the first and second AC-coupled capacitors, respectively. A third form is a differential clock signal including first and second complementary signals provided through the first and second AC-coupled capacitors, respectively.

[0008] In an exemplary configuration, the multiple mode clock receiver is implemented using N-channel and P-channel devices. The AC-coupled capacitors may be implemented using N-channel devices configured as capacitors, each having its source and drain coupled together at a respective input. In one embodiment, these N-channel devices are matched with each other. Each of the voltage dividers may be implemented

using a pair of P-channel devices, each configured as a resistor. In one embodiment, the corresponding P-channel devices forming the voltage dividers are matched. The differential amplifier may also be implemented with P-channel and N-channel devices.

[0009] In one embodiment, the N-channel devices forming the AC-coupled capacitors are sized ~~sufficiently large~~ to overcome parasitic capacitances of the P-channel devices of the voltage dividers. An additional pair of relatively weak N-channel devices may be included and coupled to the clock inputs and the voltage divider junctions to stabilize the differential amplifier in the event of clock shutdown.

[0010] An integrated circuit (IC) according to an embodiment of the present invention includes first and second input pins, first and second capacitors, first and second voltage dividers, and a differential amplifier. Each capacitor has a first end coupled to an input pin and a second end coupled to a junction of a corresponding voltage divider. The first and second capacitors include first and second N-channel devices, respectively, each having its source and a drain coupled together at the first end and a gate forming the second end; The differential amplifier has a differential input including a first input coupled to a junction of the first voltage divider and a second input coupled to the junction of the second voltage divider. The differential amplifier further has an output which provides an output clock signal that is aligned with an input clock signal provided to at least one of the first and second input pins.

[0011] In one embodiment of the IC, the first input pin is selectively coupled to either a single-ended clock signal or a first polarity of a differential clock signal. The second input pin is selectively disconnected or coupled to either one of a reference signal or a second polarity of the differential clock signal. In alternative embodiments, the IC may be operated in any one of multiple modes, including a first mode when the first input pin receives a single-ended clock signal and the second input pin is floated, a second mode when the first input pin receives a single-ended clock signal and the second input pin receives a reference signal, and a third mode when the first and second input pins receive first and second polarities of a differential clock signal. The IC may be implemented using N-channel and P-channel devices in a similar manner as described above.

[0012] A printed circuit board (PCB) according to an embodiment of the present invention includes a clock generator and a chip. The clock generator asserts a bus clock signal on one or more signal lines. The chip includes first and second clock input pins coupled to the one or more signal lines and a clock receiver. The clock receiver includes first and second AC-coupled capacitors, first and second voltage dividers, and a differential amplifier having an output providing an internal clock signal that is aligned with the bus clock signal.

[0013] The clock generator on the PCB may be implemented according to any one of multiple types. In one configuration, the clock generator provides a single-ended clock signal on one signal line provided to the first clock input pin of the chip, where the second clock input pin is left floating. In a second configuration, the clock generator further provides a reference signal on a second signal line provided to the second clock input pin of the chip. In a third configuration, the clock generator provides a differential clock signal on first and second signal lines, which are provided to the first and second clock input pins, respectively, of the chip.